MICROCONTROLLER
UNIT 1

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- OVERVIEW OF THE 8051
- 8051 MICTROCONTROLLER HARDWARE
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INTRODUCTION

- The first task to use a new computer is to become familiar with the capability of machine.
- This is learn by studying the internal architecture.
- This is used to determine the type, number, and the size of registers and other circuitry.
- This chapter provides a broad overview of the architecture of 8051.

MICROCONTROLLERS AND EMBEDDED PROCESSORS

Microcontroller vs. General-Purpose Microprocessor

- General-purpose microprocessors

Contains:

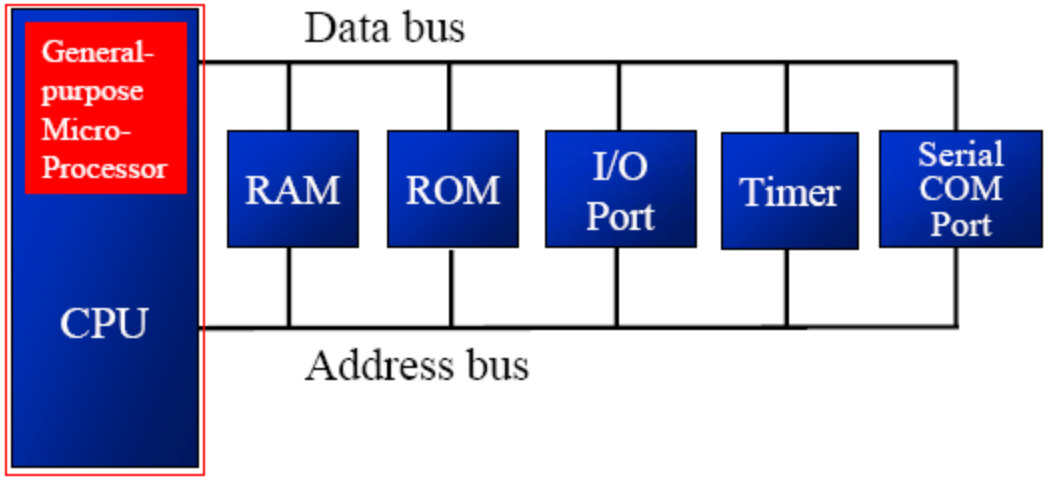
  - No RAM
  - No ROM
  - No I/O ports

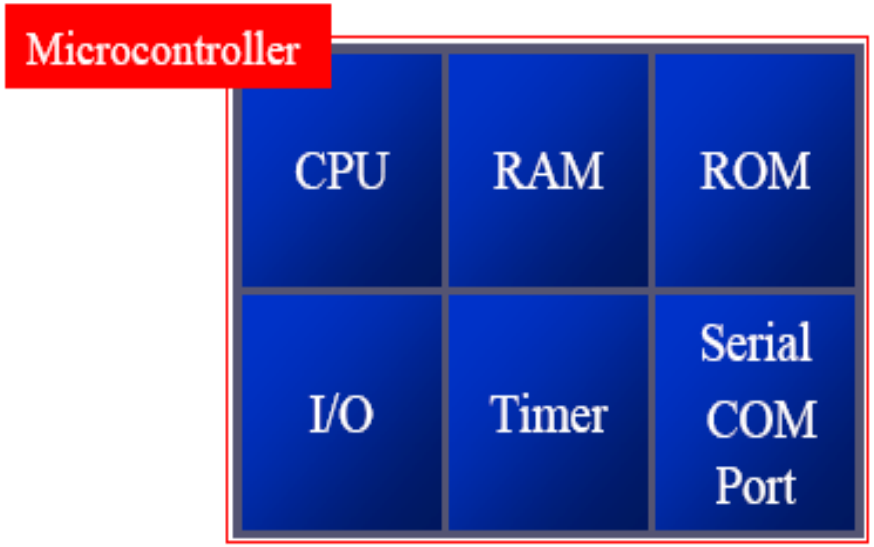
- Microcontroller has

  - CPU (microprocessor)
  - RAM
  - ROM
  - I/O ports
  - Timer
  - ADC and other peripherals

MICROCONTROLLERS AND EMBEDDED PROCESSORS

Microcontroller vs. General-Purpose Microprocessor





MICROCONTROLLERS AND EMBEDDED PROCESSORS

Microcontroller For Embedded System

- An embedded product uses a microprocessor (or microcontroller) to do one task and one task only
  - There is only one application software that is typically burned into ROM
- A PC, in contrast with the embedded system, can be used for any number of applications
  - It has RAM memory and an operating system that loads a variety of applications into RAM and lets the CPU run them
- A PC contains or is connected to various embedded products
  - Each one peripheral has a microcontroller inside it that performs only one task

OVERVIEW OF THE 8051

- Intel introduced 8051, referred as MCS-51, in 1981
- The 8051 is an 8-bit processor
  - The CPU can work on only 8 bits of data at a time
- The 8051 had:
  - 128 bytes of RAM
  - 4K bytes of on-chip ROM
  - Two timers
  - One serial port
  - Four I/O ports, each 8 bits wide
  - 6 interrupt sources
- The 8051 became widely popular after allowing other manufactures to make and market any flavor of the 8051, but remaining code-compatible

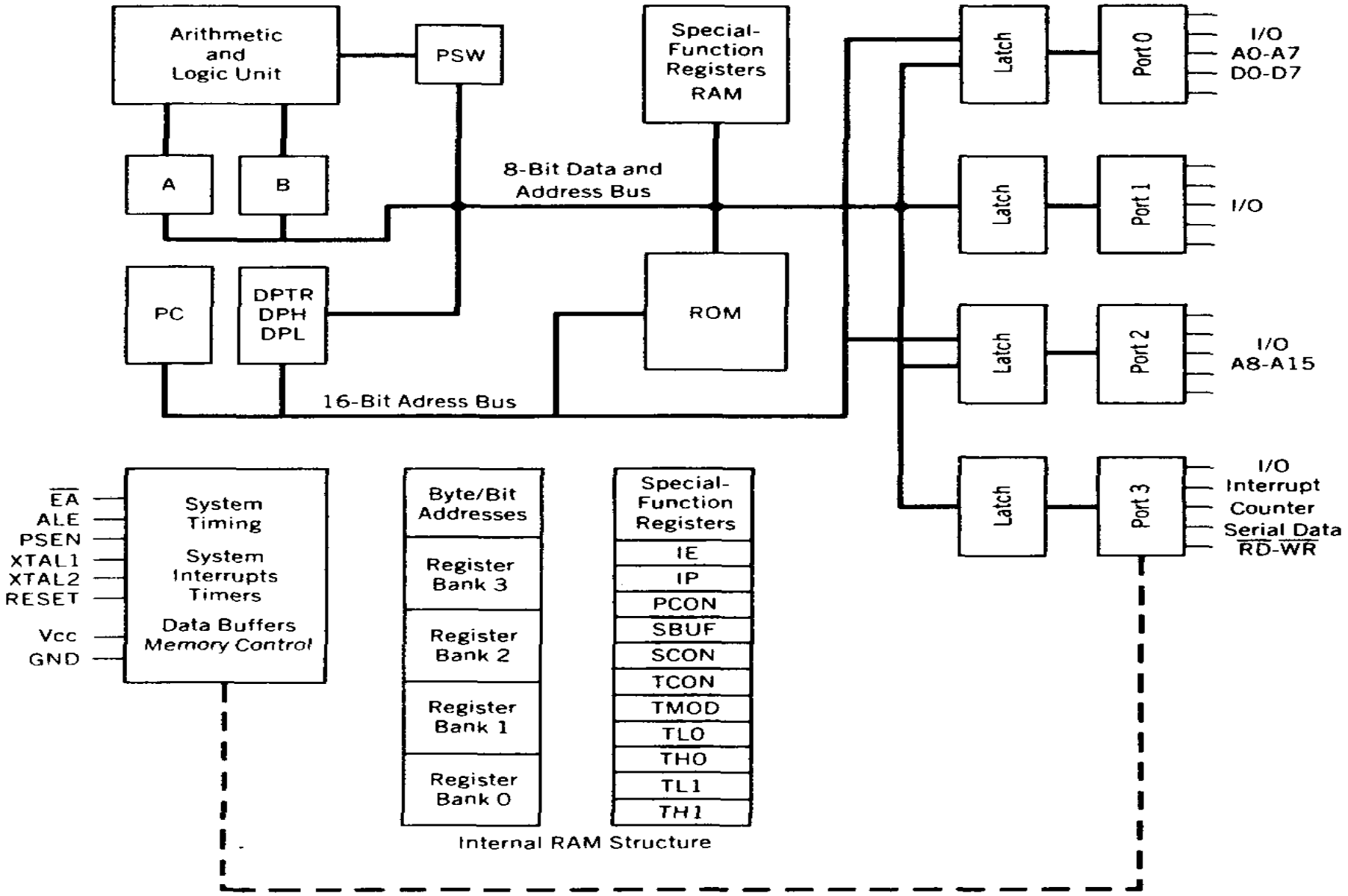
8051 MICROCONTROLLER HARDWARE

- This include a whole family of microcontroller ranging from 8031 to 8751

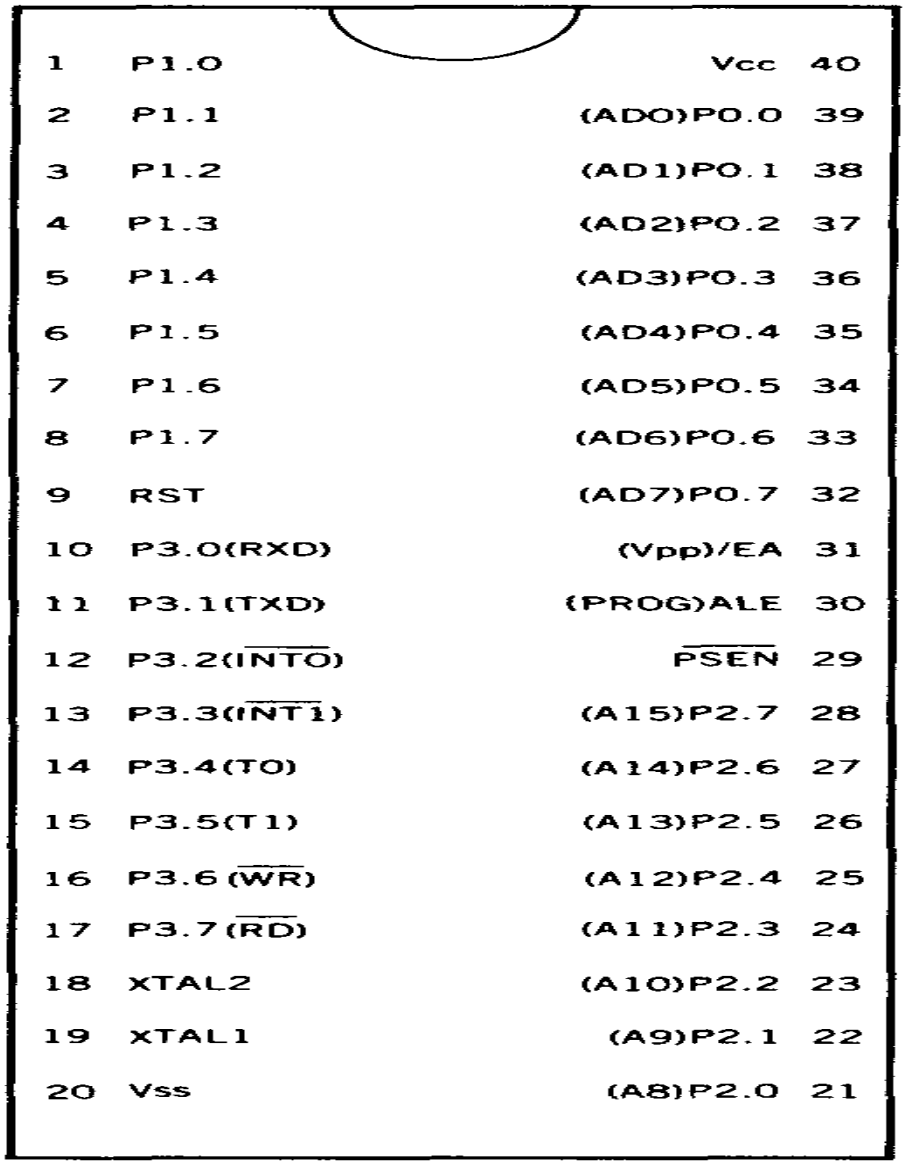
- These are available in N-channel Metal oxide silicon(NMOS) and complementary Metal Oxide Silicon(cmos) construction in variety of package type.

- 8052 is the enhance version of 8051 .

8051 BLOCK DIAGRAM

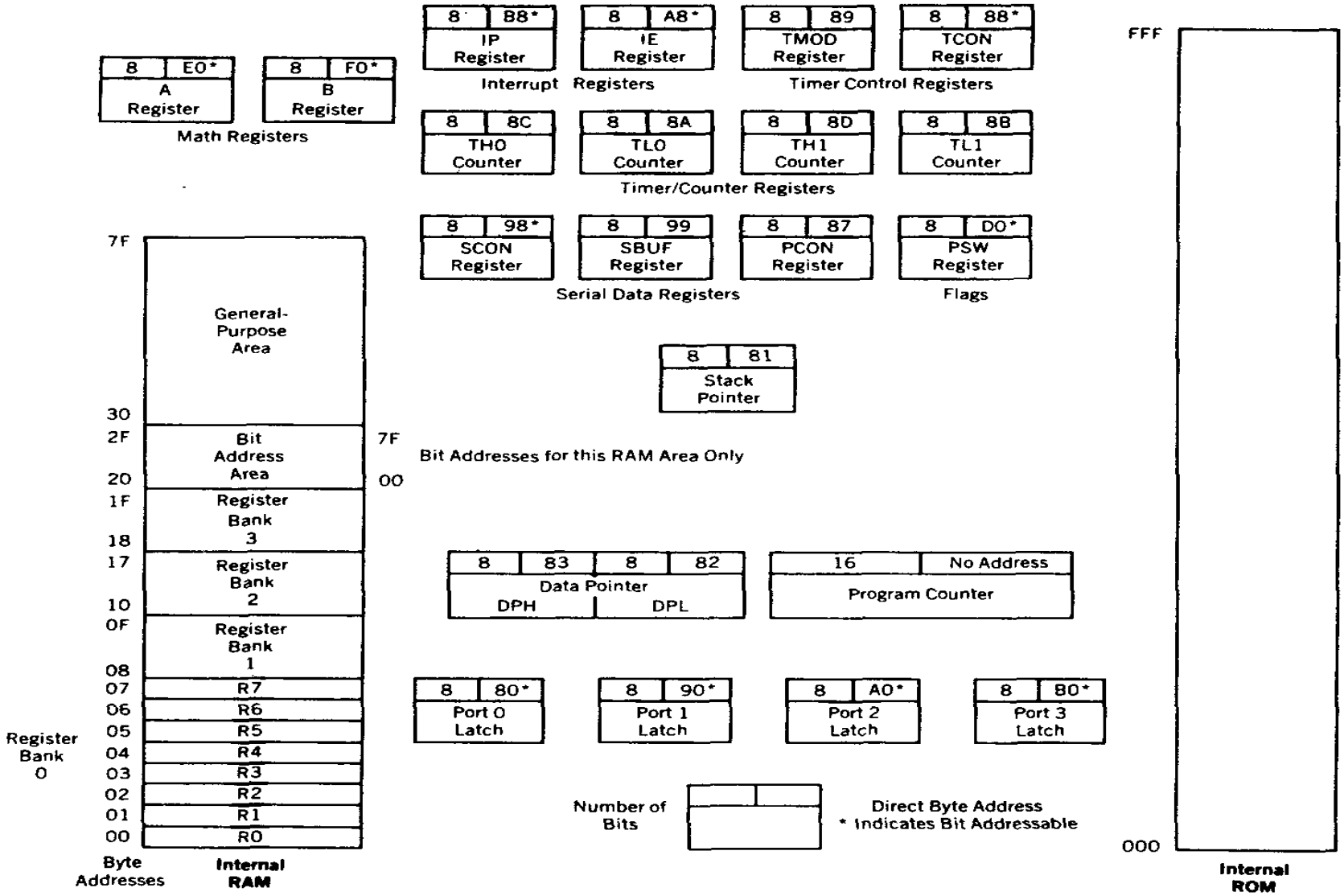


8051 DIP PIN ASSIGNMENT



Port 1 Bit 0	1	P1.0	Vcc	40	+5V
Port 1 Bit 1	2	P1.1	(AD0)P0.0	39	Port 0 Bit 0 (Address/Data 0)
Port 1 Bit 2	3	P1.2	(AD1)P0.1	38	Port 0 Bit 1 (Address/Data 1)
Port 1 Bit 3	4	P1.3	(AD2)P0.2	37	Port 0 Bit 2 (Address/Data 2)
Port 1 Bit 4	5	P1.4	(AD3)P0.3	36	Port 0 Bit 3 (Address/Data 3)
Port 1 Bit 5	6	P1.5	(AD4)P0.4	35	Port 0 Bit 4 (Address/Data 4)
Port 1 Bit 6	7	P1.6	(AD5)P0.5	34	Port 0 Bit 5 (Address/Data 5)
Port 1 Bit 7	8	P1.7	(AD6)P0.6	33	Port 0 Bit 6 (Address/Data 6)
Reset Input	9	RST	(AD7)P0.7	32	Port 0 Bit 7 (Address/Data 7)
Port 3 Bit 0 (Receive Data)	10	P3.0(RXD)	(Vpp)/EA	31	External Enable (EPROM Programming Voltage)
Port 3 Bit 1 (XMIT Data)	11	P3.1(TXD)	(PROG)ALE	30	Address Latch Enable (EPROM Program Pulse)
Port 3 Bit 2 (Interrupt 0)	12	P3.2($\overline{\text{INT0}}$)	$\overline{\text{PSEN}}$	29	Program Store Enable
Port 3 Bit 3 (Interrupt 1)	13	P3.3($\overline{\text{INT1}}$)	(A15)P2.7	28	Port 2 Bit 7 (Address 15)
Port 3 Bit 4 (Timer 0 Input)	14	P3.4(T0)	(A14)P2.6	27	Port 2 Bit 6 (Address 14)
Port 3 Bit 5 (Timer 1 Input)	15	P3.5(T1)	(A13)P2.5	26	Port 2 Bit 5 (Address 13)
Port 3 Bit 6 (Write Strobe)	16	P3.6 ($\overline{\text{WR}}$)	(A12)P2.4	25	Port 2 Bit 4 (Address 12)
Port 3 Bit 7 (Read Strobe)	17	P3.7 ($\overline{\text{RD}}$)	(A11)P2.3	24	Port 2 Bit 3 (Address 11)
Crystal Input 2	18	XTAL2	(A10)P2.2	23	Port 2 Bit 2 (Address 10)
Crystal Input 1	19	XTAL1	(A9)P2.1	22	Port 2 Bit 1 (Address 9)
Ground	20	Vss	(A8)P2.0	21	Port 2 Bit 0 (Address 8)

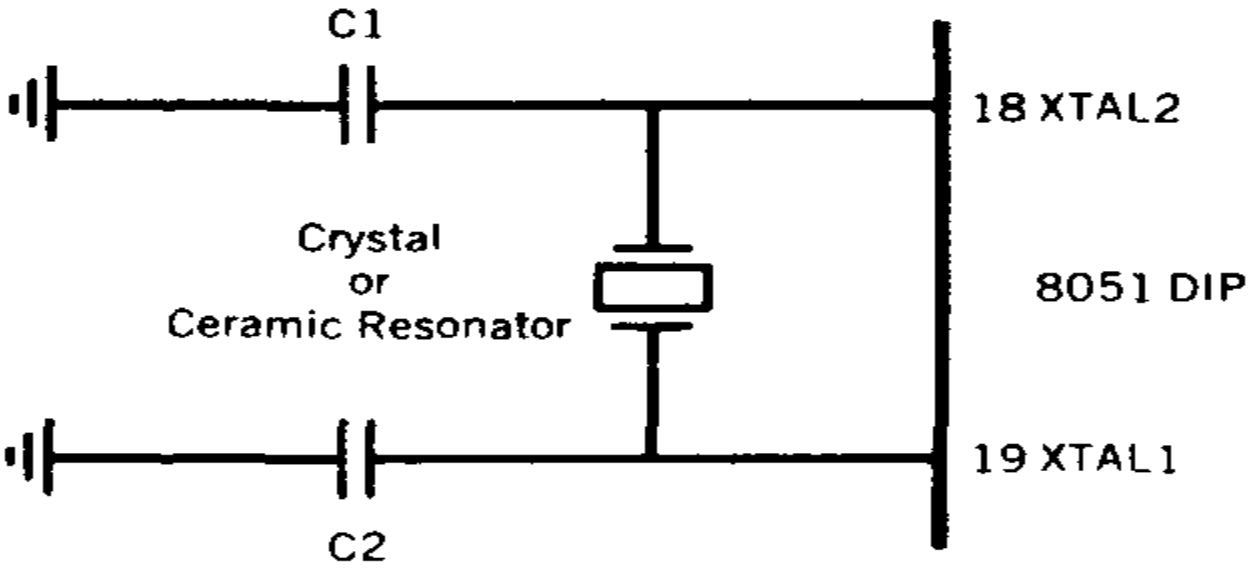
8051 PROGRAMMING MODEL

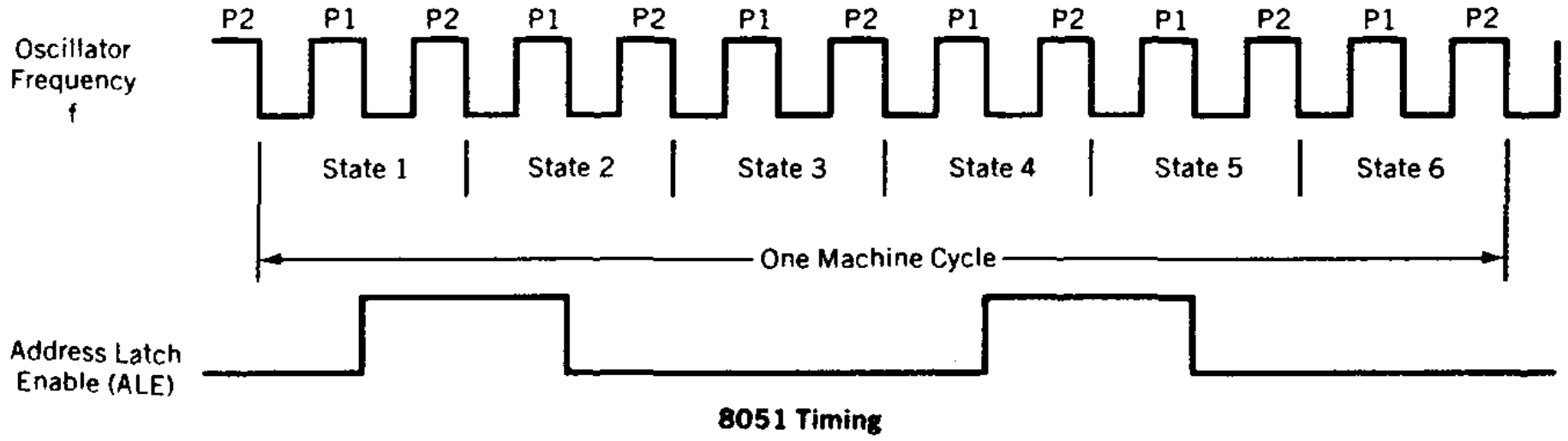


Specific feature of 8051 Architecture:

- Eight-bit cpu with register A (the accumulator) and B.
- Sixteen-bit program counter (PC) and data pointer(DPTR).
- Eight-bit stack pointer (SP).
- Internal ROM or EPROM(8751) of 0 (8031) to 4k (8051).
- Internal RAM of 128 bytes:
- Four register banks, each containing eight register.
- Sixteen bytes, which may be addressed at the bit level.
- Eight bytes of general purpose data memory.
- Thirty-two I/O pins arranged as four 8-bit ports:P0-P3.
- Two 16-bit trimmer/counter:T0-T1.
- Full duplex serial data receiver/transmitter.
- Control register : TCON , TMOD , SCON , PCON , IP and IE.
- Two external and three internal interrupt source.

OSCILLATOR CIRCUIT AND TIMING





8051 Timing

ADDRESSING MODES

- The CPU can access data in various ways, which are called addressing modes

  - Immediate
  - Register
  - Direct
  - Register indirect
  - Indexed

IMMEDIATE ADDRESSING MODE

- The source operand is a constant
  - The immediate data must be preceded by the pound sign, “#”
  - Can load information into any registers, including 16-bit DPTR register
  - MOV A,#25H ;load 25H into A
  - MOV R4,#62 ;load 62 into R4
- We can also use immediate addressing mode to send data to 8051 ports
  - MOV P1,#55H

REGISTER ADDRESSING MODE

- Use registers to hold the data to be manipulated
  - MOV A,R0 ;copy contents of R0 into A
  - MOV R2,A ;copy contents of A into R2
  - ADD A,R5 ;add contents of R5 to A
  - ADD A,R7 ;add contents of R7 to A
  - MOV R6,A ;save accumulator in R6
- The source and destination registers must match in size
  - MOV DPTR,#25F5H
  - MOV R7,DPL
  - MOV R6,DPH
- The movement of data between Rn registers is not allowed
  - MOV R4,R7 is invalid

Direct Addressing Mode:

- It is most often used the direct addressing mode to access RAM locations 30 – 7FH
  - The entire 128 bytes of RAM can be accessed
  - The register bank locations are accessed by the register names

  - MOV A,4 ;is same as
  - MOV A,R4 ;which means copy R4 into A

Register Indirect Addressing Mode:

- A register is used as a pointer to the data
  - Only register R0 and R1 are used for this purpose
  - R2 – R7 cannot be used to hold the address of an operand located in RAM
- When R0 and R1 hold the addresses of RAM locations, they must be preceded by the "@" sign

  - MOV A,@R0 ; move contents of RAM whose naddress is held by R0 into A
  - MOV @R1,B ; move contents of B into RAM whose address is held by R1

Indexed Addressing Mode:

- Indexed addressing mode is widely used in accessing data elements of look-up table entries located in the program ROM

  - The instruction used for this purpose is
    - MOVC A,@A+DPTR
    - Use instruction MOVC, “C” means code
    - The contents of A are added to the 16-bit register DPTR to form the 16-bit address of the needed data